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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,523	06/29/2001	Steven K. Hsu	884.453US1	8095

7590 05/08/2002

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EXAMINER

TRAN, ANH Q

ART UNIT	PAPER NUMBER
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2819

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Applicati n No.

09/896,523

Applicant(s)

HSU ET AL.

Examin r

Anh Q. Tran

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 March 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kumagai (5,896,043).

Regarding claim 1, Kumagai shows a voltage-level converter (Fig. 11) comprising:

A static voltage-level converter (30); and

A split-level output circuit (50) coupled to the static voltage-level converter.

Regarding claim 2, Kumagai shows the static voltage-level converter comprises:

An input node (VIN), a first output node (N1), and a second output node (VIN\*);

A first pair of transistors connected in series, the first pair of transistors including a first transistor (1) and a second transistor (3), the first transistor coupled to the input node;

A second pair of transistors connected in series, the second pair of transistors including a first transistor (2) and a second transistor (4), the second transistor of the second pair of transistors being cross-coupled with the second transistor of the first pair of transistors and the second transistor of the second pair of transistors being coupled to the first output node; and

An inverter (INV1) coupled to the input node, to the first transistor of the second pair of transistors, and to the second output node.

Regarding claim 3, Kumagai shows the split-level output circuit comprises a plurality of insulated-gate field-effect transistors (P/N-MOS transistors, col. 18).

Regarding claim 4, Kumagai shows the static voltage-level converter (30) comprises a first output node (N1) and a second output node (VIN\*) and the split-level output circuit (50) comprises a first split-level input node (N1), a second split-level input node (VIN\*), a split-level output node (VOUT), a first insulated-gate field-effect transistor (54a) coupled to the first split-level input node and a second insulated-gate FET (52a) coupled to the second split-level input node, the first insulated-gate FET being connected in series with the second insulated-gate FET, the first insulated gate FET and the second insulated gate FET having a common node coupled to the split-level output node and the first split-level input node coupled to the first output node and the second split-level input node coupled to the second output node.

Regarding claim 5, Kumagai shows the first insulated-gate field-effect transistor comprises a p-type insulated-gate field-effect transistor (p-channel MOSFET, col.18, line 29).

Regarding claim 6, Kumagai shows the second insulated-gate field-effect transistor comprises a n-type insulated-gate field-effect transistor (n-channel MOSFET, col.18, line 16).

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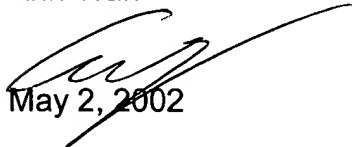
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 703-306-4507. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Anh Tran



May 2, 2002